ISSN: 2277-9655
Impact Factor: 1.852

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

Design and Analysis of Routing Algorithm for 3D Network on Chip

Prof. A. N. Shire[*1], Shilpa P. Meshram[2]
[*1,2]M.E. (Digital Electronics), Amravati university, Yavatmal, India
atul.shire@gmail.com

Abstract

Three dimensional network on chip (3D NoC) is the most thriving on chip connection architecture. According to mesh on-chip conceive approach, investigator favors mesh conceive expertise to analyzed SOCs. That is network on chip mesh architecture has been suggested as solution to address international communication trials in system on chip (SOC) architecture. The performance improvement originating from the architectural benefits of network on chip will be significantly enhanced if 3D ICs are taken up as the rudimentary fabrication methodology. By emerging 3D IC accomplish greater device integration and enhance the system presentation at smaller cost and reduces communication distance in 3D NoC. In addition to its various advantages in terms of power utilization and system performance has possibility to implement an effective architecture. In this paper, effective 3D network on chip architecture is suggested with the mechanism of congestion aware algorithm which optimizes the power utilization, system performance and minimize latency. In supplement we have integrated the reduced cost platform of 3D NoC mesh architecture which can be effectively utilized for fault tolerant and minimized traffic. Based on suggested routing for 3D NoC can help to achieve significant power utilization and minimized the latency.

Keyword: 3D IC, 3D Network on Chip, Routing Algorithm, Topology.

Introduction

The significant increase within the speed and quality of today's very-large-scale integration (VLSI) chip style has lime lighted to the time of System-on-chip (SoC) [1]. SoC is a broad construct that refers to the mixing of nearly all aspects of a system on chip. SoC often driven by the ever growing demand for inflated system practicality and compactness at minimum price, power consumption and time to plug. The Network-on-Chip (NoC) model is rising as a revolutionary methodology in resolution the performance limitations arising out of long interconnects, outperforming more thought bus architectures [2] [3] [4]. Additionally to providing a solution for the global wire delay problem, the NoC paradigm conjointly eases integration of high numbers of intellectual property (IP) cores in an exceedingly single SoC. On-chip interconnection networks or Network-on-Chip are planned as an answer to handle the global communication challenges in SoC design[2]. In NoC, segments communicate with one another by causation packetized knowledge over this network. [7]These long interconnects are quickly turning into a performance impediment in terms of communication latency and power.

The choices of the 2D integrated circuits (ICs) limit the performance enhancements arising out of NoC architectures. As 3D ICs, that contain multiple layers of active devices, have the potential for enhancing system performance [5], [6], [7], [8]. According to [6], 3D ICs provide performance enhancements even in the absence of scaling, this is often the results of the reduction in interconnect length. Besides this clear benefit, package density is enhancing considerably, power is reduced from shorter wires and electronic equipment is a lot of more immue to noise [8]. The performance improvement arising from the architectural advantages of NoCs are considerably increased if 3D ICs are adopted as the basic fabrication methodology. The amalgamation of two rising paradigms, NOC and 3D IC, allows for the creation of recent structures that change significant performance enhancements over a lot of ancient solutions. With freedom within the dimension, architectures that were not possible or preventative because of wiring constraints in coplanar ICs are currently attainable. The NoC address the network topology, the routing process and associated algorithms which offers a lot more flexibility in design choice.

In this paper, we have a tendency to characterize the performance of multiple 3D NoC architecture within the presence of realistic traffic patterns through simulation and establish the performance benchmark and related design trade-offs.

ISSN: 2277-9655
Impact Factor: 1.852

Related Work

A.3D NOC Architecture:

The generic network on- chip design as shown in Fig.1 is predicated on a consistent and scalable switch fabric network, that considers all the necessities of on-chip communications and traffic. Whenever PE represents processor element units and R represents switch fabrics (or known as router). To manage the routing messages within the network, every node contains a router to transfer the messages to the destinations. A router consists of a collection of input buffers, associate interconnect matrix, a collection of output buffers and management circuitries, that are a routing controller, associate arbiter and so on. The arbiter is intended for arbitrating over two packets that need to transverse identical path. Additionally, the router controller controls the links between input and output channels that connect this router to the neighboring routers. For routing the messages with efficiency, the algorithms of the routing controller verify the shortest methods to optimize the network performance consistent with the information of the system. Therefore, the routing algorithmic program dominates the performance of the network on-chip platforms.

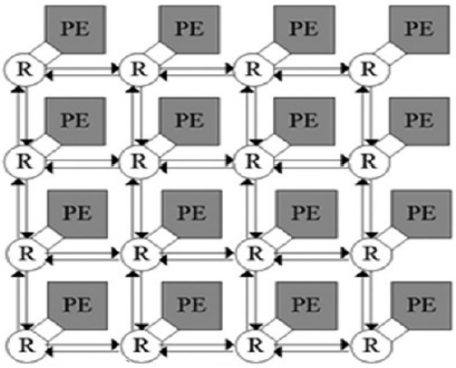

Fig 1. NOC Architecture

By combining the NOC structure with the advantages of the 3D integration lead us to present 3D-NoC as a replacement architecture as shown in fig 2. This architecture responds to the scaling demands for future SoC, exploiting the short vertical links between the adjacent layers which will clearly enhance the system performance. consistent with Feero et al [10], 3D-NoC has the flexibility to decrease the quantity of hops, a basic and necessary issue to judge the system performance.

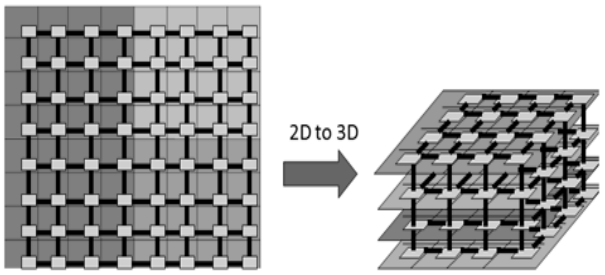

Fig 2 .3D Integration From 2D

The authors have shown that 3D ICs are power and performance economical, however once the 3D NOC is taken into consideration, the statistics are quite different. The 3D NOCs are extension to the 2D NoC architecture. for every NOC router of mesh structure, two further ports are required ensuring a 7×7 crossbar rather than 5×5 crossbar for the 2D mesh architecture. Since crossbar power will increase quadratically with the number of ports the power consumption for a 3D router is much higher than for a 2D router [11].

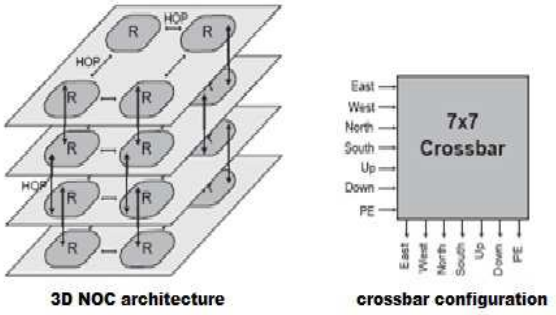

Fig 3. 3D Router 7x7 crossbar configuration

The solution to the power consumption for a 3D router has been planned by Li et al. [12]. The proposed architecture is stacked mesh design. Owing to one hop vertical communication and 6×6 routers, proposed architecture is economical enough in terms of power consumption and latency. Since the bus may be a shared medium it doesn't permit synchronous communication within the dimension. Thus, bus medium offers a enough degree of scalability for the dimension. The problem with this design is tendto improve the design to additional enhance the throughput by using the communication resources.

ISSN: 2277-9655
Impact Factor: 1.852

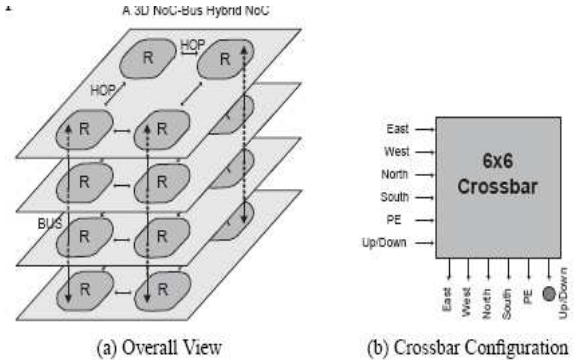

Fig 4. 3D Router 6x6 crossbar configuration

Kim et al. [14] offered an efficient router structure for 3D NOCs known as True NoC architecture within the architecture; the vertical links are embedded within the crossbar and extend to all layers. Interconnection between the assorted links during a 3D crossbar would need to be provided by dedicated association boxes at every layer. An improvement to the true 3D NOC router is planed that includes a higher energy-delay product characteristic. Despite their encouraging results, there are some vital drawbacks. Adding a large variety of vertical links during a 3D crossbar to extend NOC property leads to increased path diversity and suggests that multiple attainable ways between supply and destination pairs. It really results in a dramatic increase within the complexness and power consumption of the central arbiter. Additionally, their design can only support routing using dimension ordered routing (DOR), which is thought to suffer from poor worst-case throughput.

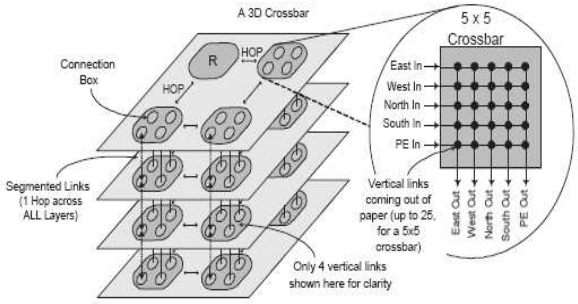

Fig 5 . 3D NoC True Router with 3D Crossbar

Based on the concept of vertical switching, Matsutani et al. [15] planned an architecture is not power-efficient, asa result of it needs massive vertical switches. Park et al. [16] projected A Multi-layered On-Chip Interconnect Router Architecture (MIRA), that is predicated on implementing a 2D mesh chip multiprocessor in three dimensions. the most important disadvantage of the design is that it assumes the processor cores are designed in 3D. This makes it tough to use existing extremely optimize 2D processor core designs.

In [17], An increased deciding routing rule to avoid congestion in 2D NOC architectures was projected. Additionally, the proposed dynamic routing approach will tolerate one link failure. Utilizing the out there communication resources, we have a tendency to enhance our approach to handle fault tolerance for inter-layer communication of stacked mesh architecture. Most of the mention architecture square measure either power economical or high performance. Symmetrical 3D NOC design is high-throughput however not power efficient. On the other hand, architectures like true NoC or stacked mesh architectures square measure power economical at the expense of reduced throughput. We tend to re-hybridize the stacked mesh design to boost system output, fault tolerance, and power potency.

B. 3D NOC Topology:

The topology of a NOC [3] specifies the physical organization of the interconnection network. It defines the interconnection between nodes, switches, and links [19]. one in all the kind of topology configuration in direct network topologies [20], every node has direct point-to-point links to a subset of alternative nodes within the system known as neighboring nodes. The nodes carries with it computational blocks and/or memories, as well as a network interface (NI) block that acts as a router. This router is connected to the router of the neighboring nodes through links. Most direct network topologies have associated orthogonal NOC topology. The topology of a NOC [20] specifies the physical organization of the interconnection network. It defines the interconnection between nodes, switches, and links [19]. one amongst the kind of configuration is that the in direct network topology [20], every node has direct point-to-point links to a set of alternative nodes within the system known as neighbor nodes. The node carries with it procedure blocks and recollection similarly as a NI block that acts as a router. This router is connected to the routers of the neighboring nodes through links. Most direct network topologies have associate orthogonal implementation, whenever the nodes are organized in associate n dimensional orthogonal area, in such the way that each link produces a displacement in a very single direction. Routing for such networks is fairly easy and may be implemented expeditiously in hardware. Samples of well-liked orthogonal direct network include the n-

ISSN: 2277-9655
Impact Factor: 1.852

dimensional mesh, torus, folded torus, hypercube and polygon topologies.

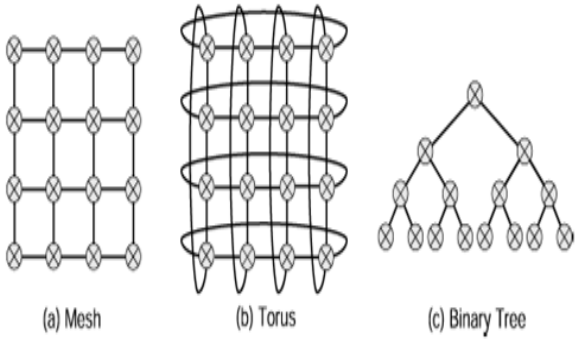

Fig 6 . Direct Network Topology

C. Routing Algorithm:

One of the important designs step that should be taken care of while conceiving a 3D NoC is the implementation of an effective routing algorithm whereas there is alarge number of complicated routing algorithm, but they could require more convoluted implementation than that of the deterministic ones. The deterministic routing algorithms have been taken up for 3D-NoC concepts. One of the well renowned and well utilized routing designs in 3D-NoCs is the Dimension order Routing (DOR) XYZ algorithm. XYZ is a easy algorithm, very easy to apply and free of deadlock [21][23]. But on the other hand, it bears from a non-efficient pipeline stage usage. This can introduce an significant effect on the router delay and finally on the scheme overall performance. Enhancing this algorithm while keeping its ease may improve the scheme performance by decreasing the packet delay.

Look up table routing algorithm is more well liked in implementation, where a look up table is stored in every mode. The routing algorithm is altered by replacing the entries of the look up table. The pseudo adaptive XY routing algorithm works in deterministic mode when mesh is congested. When mesh become impeded, the algorithm swap to the adaptive mode and start to search routes that are not congested.

In the adaptive XYZ routing[22], the main heading the fact and packets transverse depends on the position of present node and line extent of the buffer in x-direction and Y-direction as well as the response of the arbiter which will be directing the packets through the network. Adaptive routing algorithm needs more information about the network to bypass congested router in the mesh. These routing algorithms are obliviously more convoluted to apply therefore this may have more cost and power consumption.

Proposed Method for 3D NOC

In the network design of the NOC the most essential things area unit a topology and a routing algorithmic program. Routers route the packets based on the algorithm that they used. Each system has its own necessities for the routing algorithm. Routing on NOC is kind of just like routing on any network. A routing algorithm determines however the data is routed from sender to receiver. every packet has many paths to decide on, thus the performance and also the efficiency of the NOC depends on the routing algorithm.

A 3D NOC composed of many layers interconnected by vertical links is taken into account with the assumptions that the layers are and the 3D stack isn't divided. the fundamental plan of the proposed routing algorithm (shown in fig 7) is to move the message to the destination layer first. Based on the plane data from the address field of the incoming data packet, the algorithm at the start decides the destination plane. The algorithm principally concentrates on the case once the source plane (Sp) not equal to destination plane (Dp). so as to achieve the destination plane, the algorithm chooses the proximal vertical nodes among the vertical nodes available within the corresponding current plane. The message spans through the layers and reaches the destination plane. within the destination plane, the message may additionally got to move within the present layer that is completed using 2d routing. The 2D routing scheme followed is dimension order routing. The effectiveness of the scheme depends on our focus to decide on the proximal 3D node and finds a path from any source to a given destination.

ISSN: 2277-9655
Impact Factor: 1.852

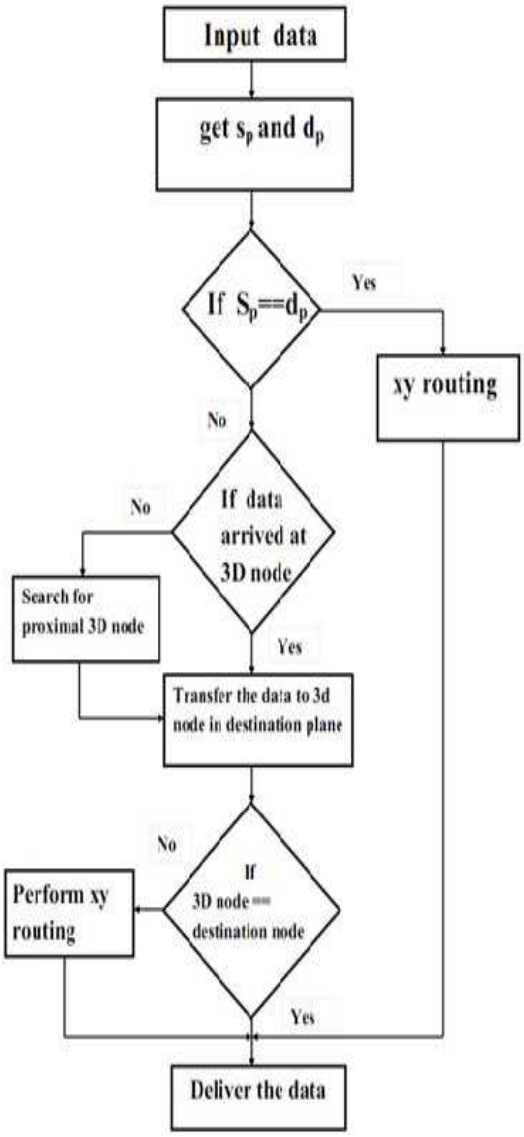

Fig 7. Proposed Algorithm

Xilinx is employed that enables creating the check bench for the coding and therefore the simulation result's verified. The propagation of the data through every node can offer information concerning the hop count needed so as to the reach the specified destination. The implementation of the routing scheme is achieved on Xilinx.

Conclusion

3D technology is envisioned to provide a performance-rich, area and energy-efficient and temperature-aware design space for SoC architectures. The networks on chips are a necessity for achieving 3D integration. In this paper, we presented 3D NoC architecture, direct network topology and the deterministic routing algorithm. This paper showed the on-chip interconnect in a 3D setting will play a crucial role in optimizing the performance, area, energy and thermal behaviors we have explored several design options for 3D NoCs, 3D integration presents the interconnect designer with several new challenges. In the future, we plan to investigate the design of a pipelined arbitration scheme to support routing within the context of fault tolerance, congestion minimization and low latency.

Acknowledgment: We acknowledge our senior faculty who has provided me their views in the selection of topic.

References

[1] Luca Benini and G. De Micheli,— Networks on chips: A new SoC paradigm,‖ computers, vol. 35, no. 1, Jan. 2002.
[2] C. Nicopoulas,Vijayakrishnan Narayanan and Chita R.Das,—Networkon-Chip architectures‖, Springer.
[3] Fayez Gebali, Haytham Elmiligi, Mohammed Watheq El - Kharaish, —Network On Chips-Theory And Practise‖..
[4] Y. Deng et al., —2.5D System Integration: A Design Driven System Implementation Schema,‖ Proc. Asia and South Pacific Design Automation Conf. (ASP-DAC), 2004.
[5] W.R. Davis et al., —Demystifying 3D ICS: The Pros and Cons of Going Vertical,‖ IEEE Design and Test of Computers, vol. 22, no. 6, Nov./Dec. 2005
[6] A.W. Topol et al., —Three-Dimensional Integrated Circuits,‖ IBM J. Research and Development, vol. 50, nos. 4/5, July-Sept. 2006
[7] H.G. Lee et al., —On-Chip Communication Architecture Exploration: A Quantitative Evaluation of Point-to-Point, Bus, and Network-on-Chip Approaches,‖ ACM Trans. Design Automation of Electronic Systems, vol. 12, no. 3, pp. 1-20, Aug. 2007.
[8] M. Ieong et al., "Three Dimensional CMOS Devices and Integrated Circuits,‖ Proc. IEEE Custom Integrated Circuits Conf. (CICC), 2003.
[9] Brett Stanley Feero,Partha Pratim Pande, -Networks-on-Chip in a Three-Dimensional Environment: A Performance Evaluation‖, IEEE TRANSACTIONS ON COMPUTERS, VOL. 58, NO. 1, JANUARY 2009
[10] B. Feero, P. Pratim Pande, Performance Evaluation for Three- Dimensional Networks-on-Chip, Proceedings of IEEE Computer

Society Annual Symposium on VLSI (ISVLSI), 9th- 11th May 2007, pp. 305-310.

[11] L. P. Carloni, P. Pande, and Y. Xie, "Networks-on-chip in emerging interconnect paradigms: Advantages and challenges,‖ in Proceedings of the International Symposium on Networks-on-Chip", 2009, pp. 93–102.

[12] F. Li, C. Nicopoulos, T. Richardson, Y. Xie, V. Narayanan, and M. Kandemir, ―Design and Management of 3D Chip Multiprocessors Using Network-in-Memory,‖ in Proceedings of the International Symposium on Computer Architecture, 2006, pp. 130–141.

[13] A.-M. Rahmani, K. Latif, V. Kameswar Rao, P. Liljeberg, J. Plosila, and H. Tenhunen, ―Congestion Aware, Fault Tolerant, and Thermally Efficient Inter-Layer Communication Scheme for Hybrid NoC-Bus 3D Architectures,‖ in Proceedings of the International Symposium on Networks-on-Chip, 2011, pp. 65 –72.

[14] J. Kim, C. Nicopoulos, D. Park, R. Das, Y. Xie, V. Narayanan, M. S. Yousif, and C. R. Das, ―A novel dimensionally-decomposed router for on-chip communication in 3D architectures,‖ in Proceedings of the International Symposium on Computer Architecture, 2007, pp. 138–149.

[15] H. Matsutani, M. Koibuchi, and H. Amano, - "Tightly-Coupled Multi-Layer Topologies for 3-D NoCs,‖ in Proceedings of the International Conference on Parallel Processing", 2007, pp. 75–84.

[16] D. Park, S. Eachempati, R. Das, A. Mishra, Y. Xie, N. Vijaykrishnan, and C. Das, ―MIRA: A Multi-layered On-Chip Interconnect Router Architecture,‖ in Proceedings of the International Symposium on Computer Architecture, 2008, pp. 251–261.

[17] P. Lotfi-Kamran, A.-M. Rahmani, M. Daneshtalab, A. Afzali- Kusha, and Z. Navabi, - EDXY - A low cost congestion-aware routing algorithm for network-on-chips,‖ Journal of Systems Architecture, vol. 56, no. 7, pp. 256–264, 2010.

[18] S. Lin, T. Yin, H. Wang, and A. Wu, ―Traffic- and thermal-aware routing for throttled three-dimensional Network-on-Chip systems,‖ in Proceedings of the Internation

[19] Qiaoyan Yu, Student Member,IEEE, and Paul Ampadu,Member,IEEE. ―A Flexible Parallel Simulator for Networks - on - Chip with Error Control‖, ieee transactions on computer-aided design of integratedcircuits and systems, vol. 29, no. 1, january 2010.

[20] M. E. G´ omez, J. Flich, P. L´opez, A. Robles, and J. Duato N. A. Nordbotten, O. Lysne, and T. Skeie, ―An Effective Fault –Tolerant Routing Methodology for Direct Networks‖,Proceedings of the 2004 International Conference on Parallel Processing 2004, IEEE.

[21] C. H. Chao, K. Y. Jheng, H. Y. Wang, J. C. Wu, and An-Yeu Wu, ‖Traffic- and thermal-aware run-time thermal management scheme for 3D NoC systems,‖ in Proc. ACM/IEEE Int. Symp. Networks-on-Chip (NoCS), Grenoble, France,pp. 223-230, May 2010.

[22] Amir-Mohammad Rahmani, Student Member, IEEE, ―High-Performance and Fault-Tolerant 3DNoC-Bus Hybrid Architecture Using ARB-NET Based Adaptive Monitoring Platform‖ IEEE TRANSACTIONS ON COMPUTERS, VOL. XX, NO. X, OCTOBER 2011 (NOCS SPECIAL SECTION)

[23] Abbas Sheibanyrad, Maryam Bahmani ―A Deadlock-Free Distributed Routing Algorithm for Vertically Partially Connected 3D-NoCs‖, IEEE TRANSACTIONS ON COMPUTERS, VOL. 62, NO. 3, MARCH 2013.